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Implementation of Four Stage Pipeline on FPGA Platform

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ABSTRACT

PLC (Programmable Logic Controller) is used in industrial process-control applications. PLC contains a CPU core surrounded by memory and I/O peripheral devices. Most of the commercial PLCs available in market uses general purpose processor as PLC CPU. The general purpose CPU is not suitable for PLC in terms of cost and speed. This paper proposes an Instruction List (IL) processor compatible with IEC 61131-3 standards. Instruction List is a simple textual programming method for programming of PLC, given by International Electro-Techno Commission. As the program of PLC becomes more complex, the execution time taken by the PLC also increases resulting in failure in responding to high speed safety critical logic. In conventional PLC's the control specification first converted into instruction set listing that the operating systems can understand. Now a days it is becoming a standard practice to include safety critical function and operation control functions with single ladder diagram programming. Because of this, rungs in the ladder diagram increases and ultimately its performance in terms of speed decreases. For high speed safety critical application the execution time becomes critical. In this paper, a Four-stage pipeline is proposed so that each instruction is executed in single machine cycle, providing high execution speed required in many high speed and safety critical applications.

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I. INTRODUCTION

Programmable Logic Controllers are widely used in the industrial automation applications. Now-a-days it is a standard practice to include safety critical functions in PLC programming. Also, MEMS based sensors are used in the PLC applications which gives input to the PLC which is very fast changing. The processors used as PLC core are mostly general purpose processors which fail to perform when very high speed of execution is required. It is desired that processors should be dedicated to PLC tasks, rather than being general purpose and it should employ some technique such as instruction pipelining so as to speed-up the execution of PLC program. Also, the overhead routines should be less in the PLC operations. When this is achieved, PLC can respond to very fast changing inputs. Hence, to achieve fast response from the PLC, it is proposed to design a PLC dedicated Instruction List (IL) processor.In industries where PLC are used to replace the PLC Ladder logic. In industries PLC has various cards line ADC which gives data stream in digital format. We need to process digital data and execute logic using single cycle instruction list processor.

PLC uses a relay logic or if this then that line execution. But this is not always able to model complex steps hence any complex execution and multiple step latency is more. But by single cycle instruction list processor instructions like AND,OR,ST,LD,MOV,SHIFT etc. which can execute logic in single cycle. If we need complex processing the PLC uses multistep so by using single cycle instruction list, we are doing complex processing single cycle.This paper is to find replacement to plc ladder logic. We are going to implement four stage pipeline architecture. By implementing pipeline we will try to reduce latency and do complex processing in single cycle.

II. LITERATURE SURVEY

In 2000, Jan Gray [1] proposed the complete design of a simple FPGA RISC 16- bit processor core and system-on-a-chip in synthesizable Verilog. It defines a RISC instruction set architecture and then describes how to implement every part of the processor along with the design and implementation of the on-chip RAM, peripheral bus, and all peripherals. The FPGA-specific issues like available resource and synthesizability and optimizations are suggested. Wherever possible, published frequency in slowest speed grade of device is used.

In 2008, M. Chmiel[2] proposed a hardware solution for supporting effective operation of CPU of PLC. The response time of PLC was reduced by virtue of Dual Core bit-byte CPU. This architecture completely separates the bit-operations and byte operations of the CPU as well as of I/O devices, so as to reduce the input-output operation time and hence the response time of PLC. The result of the design is significant increase in the speed of bit-byte central unit. Most of the operations are bit-operations and thus, large gains are achieved through separate bit-processing, which is done independent of byte-processing.

In 2011, M. Chmiel, J. Mocha, E. Hrynkiewicz, A. Milik[3], presented an approach to the design and construction of central processing units for programmable logic controllers implemented in a FPGA development platform. Presented units are optimized for minimum response and throughput time. The CPU structure is based on bit-word architecture and two types of control data exchange methods: with handshaking – control data are passed through the two flip-flop units with acknowledgement; without handshaking – control data are passed through the dual port RAM. Third unit – simple one processor – built to compare with the above two. The paper presents specific timers/counters hardware construction solution. The architecture has its own instruction list with dedicated assembler.

III.PROBLEM STATEMENT

Programmable Logic Controllers are widely used in the industrial automation applications. Now-a-days it is a standard practice to include safety critical functions in PLC programming. Also, MEMS based sensors are used in the PLC applications which gives input to the PLC which is very fast changing.

The processors used as PLC core are mostly general purpose processors which fail to perform when very high speed of execution is required. It is desired that processors should be dedicated to PLC tasks, rather than being general purpose and it should employ some technique such as instruction pipelining so as to speed-up the execution of PLC program. Also, the overhead routines should be less in the PLC operations. When this is achieved, PLC can respond to very fast changing inputs.

Hence, to achieve fast response from the PLC, it is proposed to design a PLC dedicated Instruction List (IL) processor.

IV.OBJECTIVE

Design of IEC 61131-3 compatible Instruction List processor, with a four-stage pipeline. Implementation of IL processor on FPGA platform.

V. METHODOLOGY

3.1 Block Diagram

There are three functional units separated by the pipeline registers.

-An Instruction is fetched from the fetch unit and decoded by decode unit to interpret how is it to be executed.

-Decode unit then generates some signals which are further used by execution unit to carry out the execution of the instruction.

-Pipeline registers isolate the functional units while bringing simultaneity in their operation i.e. all functional blocks are working in parallel on different instructions.

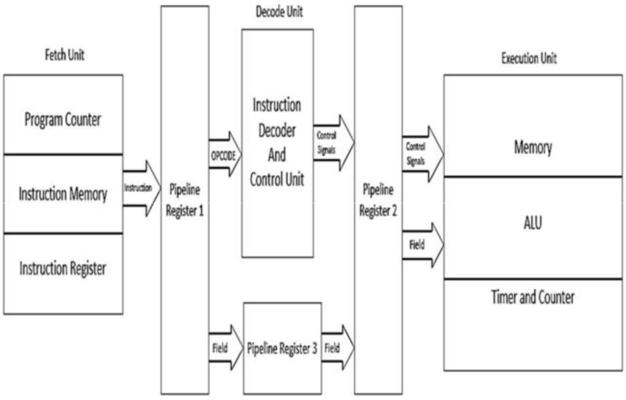


Fig. 1 Block Diagram.

The International Electro-technical Commission has defined standards for the programmable logic controllers, in the IEC 61131 suite. It has standardized five programming languages for PLC programming: Instruction List, Structured Text, Ladder Diagram, Function Blok Diagram, and Sequential Function Chart. One of these languages can be used to program a PLC.

The 'Instruction List' is a textual language which resembles the assembly language. It is used when compact size PLC programs are required, which takes less execution time. The IL is chosen as programming language for the proposed processor.

V. TEST AND RESULTS

The proposed IL processor design is synthesized using Xilinx Synthesis Tool (XST). The Xilinx ISE v12.3 as the development environment. The RTL schematic of the overall design is shown in Figure 2.

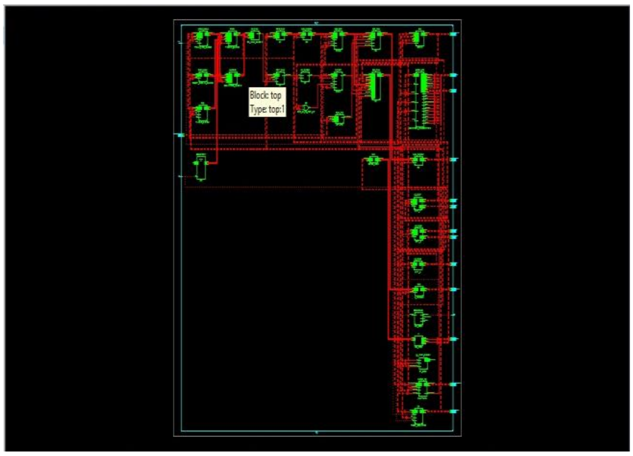
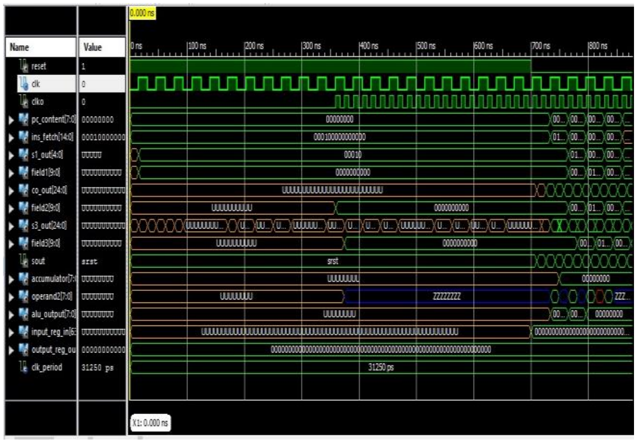


Fig. 2 RTL Schematic

The IL processor design is simulated by providing reset, clock and inputs through the VHDL test-bench. The result of the simulation are shown in Figure 3.



Name	Value
reset	1
clk	0
clko	0
pc_content[7:0]	00000000
ins_fetch[14:0]	00010000000
s1_out[4:0]	UUUUU
field1[9:0]	UUUUUUUUUU
co_out[24:0]	UUUUUUUUUUU
field2[9:0]	UUUUUUUUUU
s3_out[24:0]	UUUUUUUUUUU
field3[9:0]	UUUUUUUUUU
sout	srst
accumulator[7:0	UUUUUUUU
operand2[7:0]	UUUUUUUU
alu_output[7:0]	UUUUUUUU
input_reg_in[63	UUUUUUUUUUU
output_reg_ou	00000000000
clk_period	31250 ps

Fig. 3 Simulation Results

VI. Conclusions

The simulation of four stage pipeline on the Xilinx v12.3 with the help of appropriate test bench at the frequency of 180Mhz ,one cycle is executed in 5.28 ns is observed. For the execution of one instruction in four stage requires 1.6 ns at 64Mhz with the help of DCM(Digital Clock Manager, utility provided by Xilinx). This processor is ported on FPGA to get high speed. The instruction set of proposed IL processor is dedicated to PLC operations. Also, a four-stage instruction pipeline is employed so that execution speed is boosted-up and the PLC can responds to the fast changing inputs in high speed applications.

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